Electronic Version
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Claims

[c1] A complementary source follower circuit comprising
(A) an N-channel transistor and a P-channel transistor on a substrate, each having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal;
(B) a control signal line connection from each of said gate terminals to an input terminal;
(C) a control signal line connection from each of said source terminals to an output terminal;
(D) a connection from the drain terminal of said N-channel transistor to a positive terminal of a power supply and a connection from the drain terminal of said P-channel transistor to a negative terminal of a power supply; and
(E) a control signal line connection from a back bias control circuit to each body terminal and to each source terminal, where said back bias control circuit shifts the threshold voltage of at least one of said transistors, wherein there is no control signal line connection from a body terminal to a source terminal, from a body terminal to a drain terminal, or from said back bias circuit to a

drain terminal.

[c2] A complementary source follower circuit according to Claim 1 wherein said substrate is an SOI.

[c3] A complementary source follower circuit according to Claim 1 wherein said substrate is single crystal silicon.

[c4] A complementary source follower circuit according to Claim 3 wherein said substrate is N-doped.

[c5] A complementary source follower circuit according to Claim 3 wherein said substrate is P-doped.

[c6] A complementary source follower circuit according to Claim 3 wherein said substrate is undoped.

[c7] A complementary source follower circuit according to Claim 1 wherein at least some of the signals to said input terminal are analog.

[c8] A complementary source follower circuit according to Claim 1 that includes a level voltage shift circuit for shifting the input voltage to at least one of said transistors.

[c9] A complementary source follower circuit according to Claim 1 wherein said back bias control circuit independently shifts the threshold voltage of each of said tran-

sistors.

[c10] A complementary source follower circuit according to Claim 9 wherein said back bias control circuit shifts the threshold voltage of at least one transistor to achieve linearity when said complementary source follower circuit is in active mode.

[c11] A complementary source follower circuit according to Claim 9 wherein said back bias control circuit shifts the threshold voltage of at least one transistor to achieve non-linearity when said complementary source follower circuit is in standby mode.

[c12] A method of eliminating a dead gap in a complementary source follower circuit according to Claim 1 comprising shifting the threshold voltage of at least one of said transistors to achieve linearity when said complementary source follower circuit is in active mode.

[c13] A method according to Claim 12 wherein power loss in standby mode is reduced by shifting the threshold voltage of at least one of said transistors to create a dead gap when said complementary source follower circuit is in standby mode.

[c14] An LSI having thereon at least one complementary source follower circuit according to Claim 1.

[c15] An LSI according to Claim 14 wherein at least one complementary source follower circuit functions as an output buffer.

[c16] A complementary source follower circuit for processing an analog signal comprising
(A) an N-channel type transistor and a P-channel transistor on a substrate, each having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal, where there is no connection from a body terminal to a source terminal or from a body terminal to a drain terminal;
(B) a control signal line connection from each of said gate terminals to an input terminal;
(C) a control signal line connection from each of said source terminals to an output terminal;
(D) a connection from the drain terminal of said N-channel transistor to a positive terminal of a power supply and a connection from the drain terminal of said P-channel transistor to a negative terminal of a power supply; and
(E) a control signal line connection from a back bias control circuit to each body terminal and to each source terminal, where said back bias control circuit independently shifts the threshold voltage of each of said transistors to

achieve linearity when said complementary source follower circuit is in active mode and to achieve non-linearity when said complementary source follower circuit is in standby mode, and there is no control signal line connection from said back bias circuit to a drain terminal.

[c17] A complementary source follower circuit according to Claim 16 wherein said substrate is an SOI.

[c18] A complementary source follower circuit according to Claim 16 wherein said substrate is single crystal silicon.

[c19] A source follower circuit comprising
(A) a transistor having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal, where there is no connection from a body terminal to a source terminal or from a body terminal to a drain terminal;
(B)a control signal line connection from said gate terminal to an input terminal;
(C) a resistance load having a first terminal and a second terminal;
(D) a control signal line connection from said source terminal and from said first terminal to an output terminal;
(E) a power supply having two terminals;

(F) a connection from the drain terminal of said transistor to one terminal of said power supply and a connection from said second terminal to the other terminal of said power supply; and
(G) a control signal line connection from a back bias control circuit to said body terminal and to said source terminal, where said back bias control circuit independently controls the threshold voltage of said transistor to reduce power usage by said circuit, and there is no control signal line connection from said back bias circuit to a drain terminal.

[c20] A source follower circuit according to Claim 19 wherein said transistor is an N-channel transistor.

[c21] A source follower circuit according to Claim 1 wherein said back bias control circuit alternatively applies the voltages of Vss or Vcc to each body terminal.